

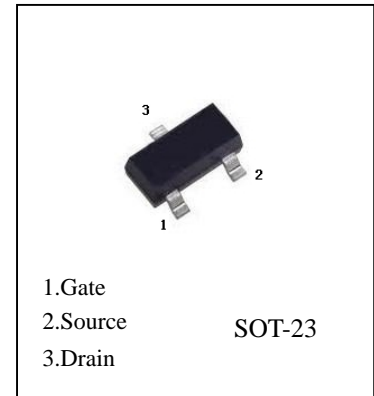
CURRENT 5.8 Ampere  
 VOLTAGE RANG 30 Volts

**AO3400**

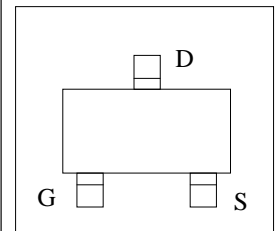
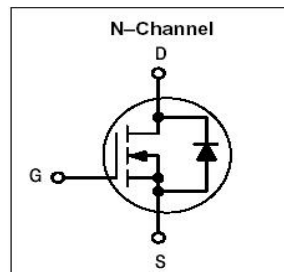
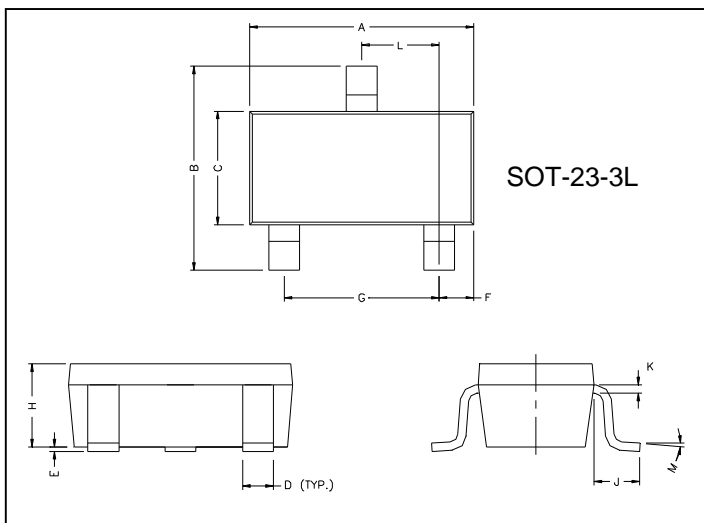
**VDS= 30V**  
**RDS(ON), Vgs@10V, Ids@5.8A < 28mΩ**  
**RDS(ON), Vgs@4.5V, Ids@5.0A < 33mΩ**  
**RDS(ON), Vgs@2.5V, Ids@4.0A < 52mΩ**

**Features**

Advanced trench process technology  
 High Density Cell Design For Ultra Low On-Resistance



**Package Dimensions**



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	1.90	REF.
B	2.65	2.95	H	1.00	1.30
C	1.50	1.70	K	0.10	0.20
D	0.35	0.50	J	0.40	-
E	0	0.10	L	0.85	1.15
F	0.45	0.55	M	0°	10°

**Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)**

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 12		
Continuous Drain Current	I <sub>D</sub>	5.8	A	
Pulsed Drain Current	I <sub>DM</sub>	30		
Maximum Power Dissipation	P <sub>D</sub>	TA = 25°C	1.4	W
		TA = 75°C	1	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	
Junction-to-Ambient Thermal Resistance (PCB mounted)	R <sub>θJA</sub>	145	°C/W	

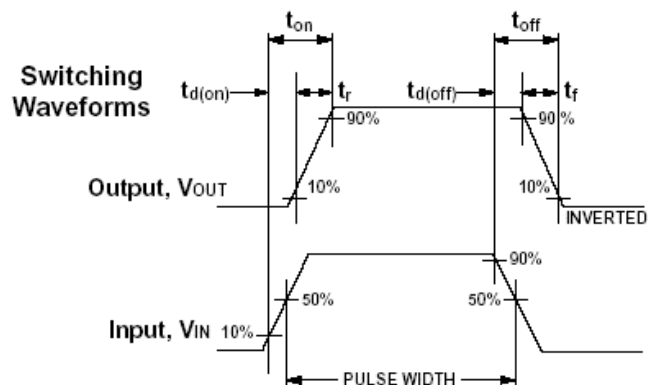
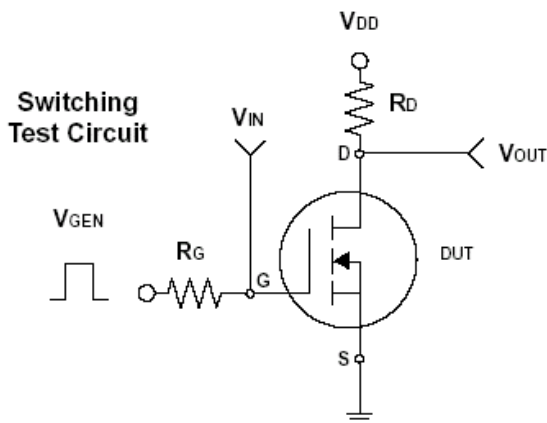
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ELECTRICAL CHARACTERISTICS (TA = 25oC unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	30			V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.8A		22.0	28.0	mΩ
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A		27.0	33.0	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 4A		43.0	52.0	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	0.7		1.4	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	uA
Gate Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 12V, V <sub>DS</sub> = 0V			±100	nA
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 5A	10	15	—	S
Gate Resistance	R <sub>g</sub>	F=1.0MHz	6	7	7.5	Ω
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 5.8A V <sub>GS</sub> = 4.5V		11	14	nC
Gate-Source Charge	Q <sub>gs</sub>			1.6		
Gate-Drain Charge	Q <sub>gd</sub>			2.8		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15V, RL=2.7Ω I <sub>D</sub> = 1A, V <sub>GEN</sub> = 10V R <sub>G</sub> = 3Ω		7	11	ns
Turn-On Rise Time	t <sub>r</sub>			15	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			38	50	
Turn-Off Fall Time	t <sub>f</sub>			3	10	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V f = 1.0 MHz		340		pF
Output Capacitance	C <sub>oss</sub>			115		
Reverse Transfer Capacitance	C <sub>rss</sub>			33		
<b>Source-Drain Diode</b>						
Max. Diode Forward Current	I <sub>S</sub>				1.6	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.6A, V <sub>GS</sub> = 0V			1.2	V

Note: Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%



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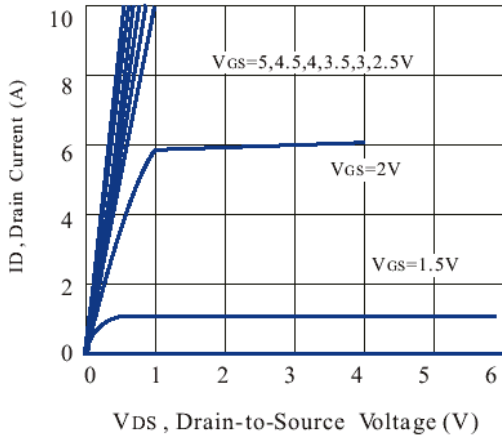


Figure 1. Output Characteristics

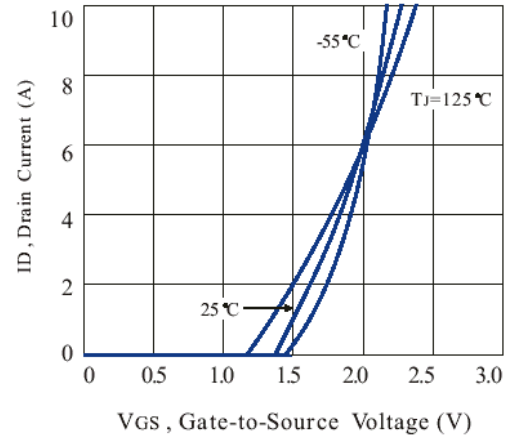


Figure 2. Transfer Characteristics

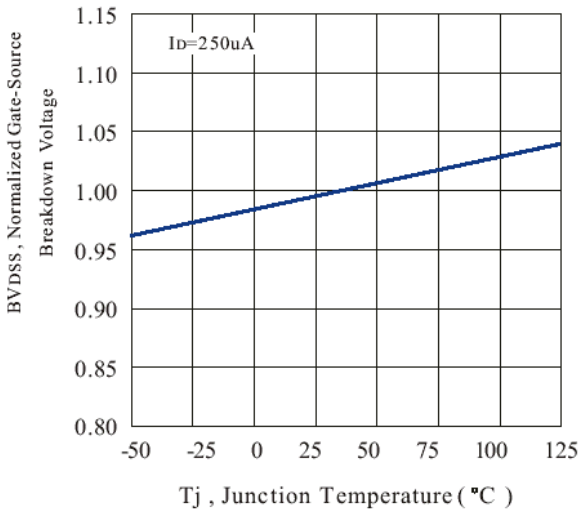


Figure 3. Breakdown Voltage Variation with Temperature

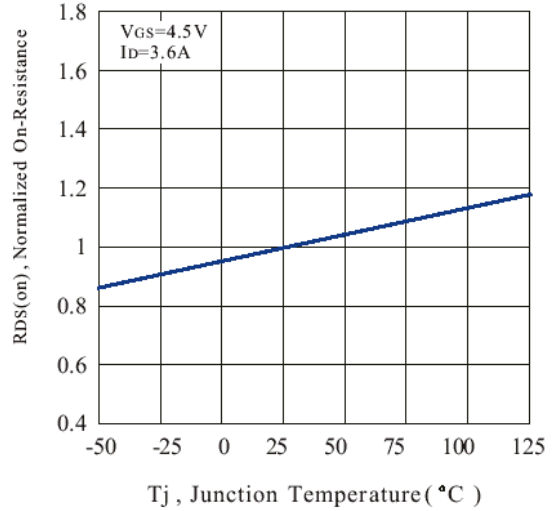


Figure 4. On-Resistance Variation with Temperature

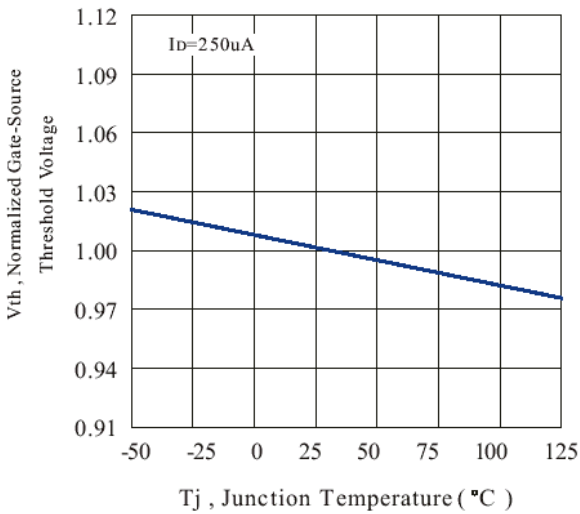


Figure 5. Gate Threshold Variation with Temperature

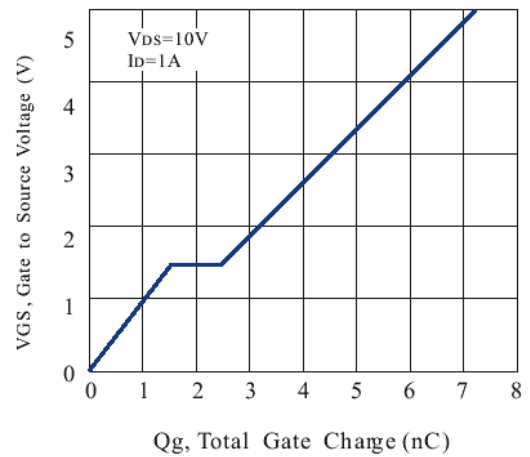


Figure 6. Gate Charge